CY7C603xx

enCoRe™ III Low Voltage

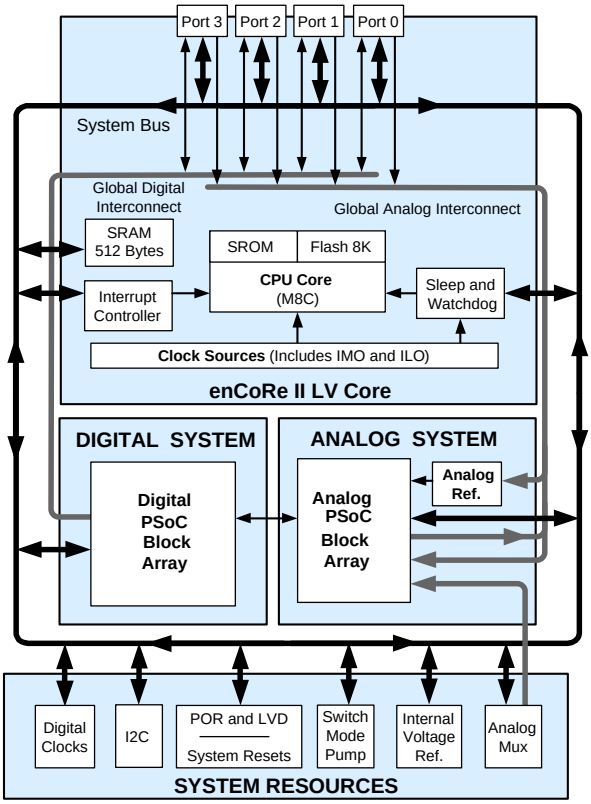
Features

- Powerful Harvard Architecture Processor
  - M8C Processor speeds to 12 MHz
  - Low power at high speed
  - 2.4V to 3.6V Operating Voltage
  - Operating Voltages down to 1.0V using On-Chip Switch Mode Pump (SMP)
  - Commercial Temperature Range: 0°C to +70°C
- Configurable Peripherals
  - 8-Bit Timers/Counters/PWM
  - Full Duplex Master or Slave SPI
  - 10-bit ADC
  - 8-bit Successive Approximation ADC
  - Comparator
- Flexible On-Chip Memory
  - 8K Flash Program Storage 50,000 Erase/Write Cycles
  - 512 Bytes SRAM Data Storage
  - In-System Serial Programming (ISSP)
  - Partial Flash Updates
  - Flexible Protection Modes
  - EEPROM Emulation in Flash
- Complete Development Tools
  - Free Development Software (PSoC Designer™)
  - Full-Featured, In-Circuit Emulator and Programmer
  - Complex Breakpoint Structure
  - 128K Trace Memory
- Precision, Programmable Clocking
  - Internal ±2.5% 24-/48-MHz Oscillator
  - Internal Oscillator for Watchdog and Sleep
- Programmable Pin Configurations
  - 10 mA Drive on all GPIO
  - Pull up, Pull down, High Z, Strong, or Open Drain Drive Modes on all GPIO
  - Up to 8 Analog Inputs on GPIO
  - Configurable Interrupt on all GPIO
- Versatile Analog Mux
  - Common Internal Analog Bus
  - Simultaneous connection of IO combinations
- Additional System Resources
  - I^2C Master, Slave and Multi-Master to 400 kHz
  - Watchdog and Sleep Timers
  - User-configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference

Applications

- Wireless mice
- Wireless gamepads
- Wireless Presenter tools
- Wireless keypads
- PlayStation® 2 wired gamepads
- PlayStation 2 bridges for wireless gamepads
  - Applications requiring a cost effective low voltage 8-bit microcontroller.

Block Diagram



enCoRe III Low Voltage Functional Overview

The enCoRe III Low Voltage (enCoRe III LV) CY7C603xx device is based on the flexible PSoC® architecture. This supports a simple set of peripherals that can be configured to match the needs of each application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts.

This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. A fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in both 28-pin SSOP and 32-pin QFN packages.

The enCoRe III LV architecture, as shown in Figure 1, consists of four main areas: the enCoRe III LV Core, the System Resources, Digital System, and Analog System. Configurable global bus resources allow combining all the device resources into a complete custom system. Each enCoRe III LV device supports a limited set of digital and analog peripherals. Depending on the package, up to 28 general purpose IOs (GPIOs) are also included. The GPIOs provide access to the global digital and analog interconnects.

enCoRe III LV Core

The enCoRe III LV core is a powerful engine that supports a rich feature set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low-speed oscillator).

The CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a four MIPS 8-bit Harvard architecture microprocessor. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

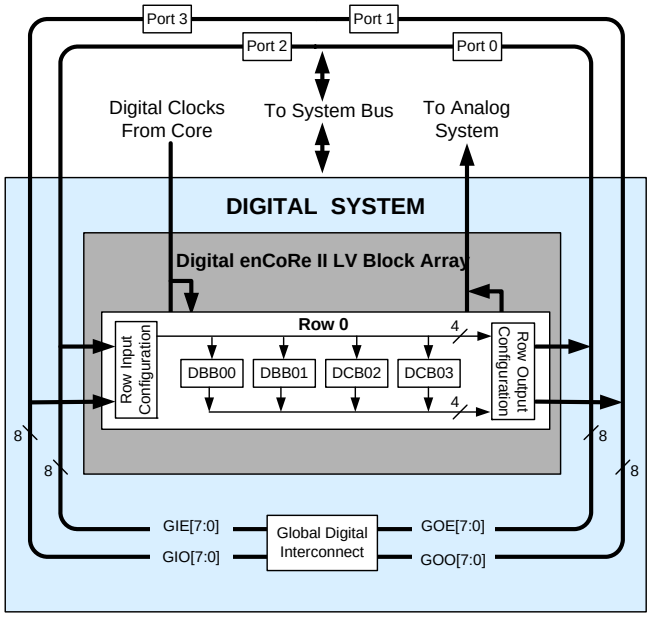
System Resources provide additional capability, such as digital clocks to increase flexibility, I2C functionality for implementing an I2C master, slave, MultiMaster, an internal voltage reference that provides an absolute value of 1.3V to a number of subsystems, a switch mode pump (SMP) that generates normal operating voltages off a single battery cell, and various system resets supported by the M8C.

The Digital System

The Digital System consists of 4 digital enCoRe III LV blocks. Each block is an 8-bit resource. Digital peripheral configurations include the following:

- PWM usable as Timer/Counter
- SPI master and slave
- I2C slave and multi-master
- CMP
- ADC10
- SARADC

Figure 1. Digital System Block Diagram



The digital blocks may be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

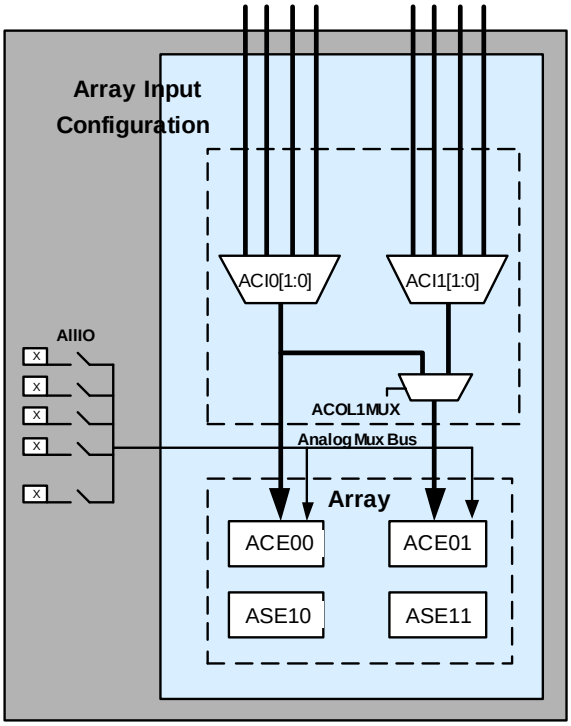
The Analog System

The Analog System consists of two configurable blocks. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the common analog functions for this device (available as user modules) are:

- Analog-to-digital converters (single with 8-bit resolution)
- Pin-to-pin comparators
- Single-ended comparators with absolute (1.3V) reference
- 1.3V reference (as a System Resource)

Analog blocks are provided in columns of two, which includes one CT (Continuous Time - ACE00 or ACE01) and one SC (Switched Capacitor - ASE10 or ASE11) blocks.

Figure 2. Analog System Block Diagram



The Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a switch mode pump, low voltage detection, and power on reset. Brief statements describing the merits of each system resource follow.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks may be generated using digital blocks as clock dividers.
- The I2C module provides 100 kHz and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 voltage reference provides an absolute reference for the analog system.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2V battery cell, providing a low-cost boost converter.
- Versatile analog multiplexer system.

enCoRe III LV Device Characteristics

The enCoRe III LV devices have four digital blocks and four analog blocks. Table 1 lists the resources available for specific enCoRe III LV devices.

Table 1. enCoRe III LV Device Characteristics

Part Number	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY7C60323 -PVXC	24	1	4	24	0	2	4	512 Bytes	8K
CY7C60323 -LFXC	28	1	4	28	0	2	4	512 Bytes	8K
CY7C60333 -LFXC	28	1	4	26	0	2	4	512 Bytes	8K

Getting Started

The quickest path to understanding the enCoRe III LV silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the enCoRe III LV and presents specific pin, register, and electrical specifications. enCoRe III LV is based on the architecture of the CY8C21x34. For in-depth information, along with detailed programming information, refer to the *PSoC Mixed-Signal Array Technical Reference Manual*, which is available at http://www.cypress.com/psoc.

For up-to-date Ordering, Packaging, and Electrical Specification information, refer to the latest device data sheets on the web at http://www.cypress.com.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, **C** compilers, and all accessories for enCoRe III LV development. Go to the Cypress Online Store web site at http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *USB (Universal Serial Bus)* to view a current list of available items.

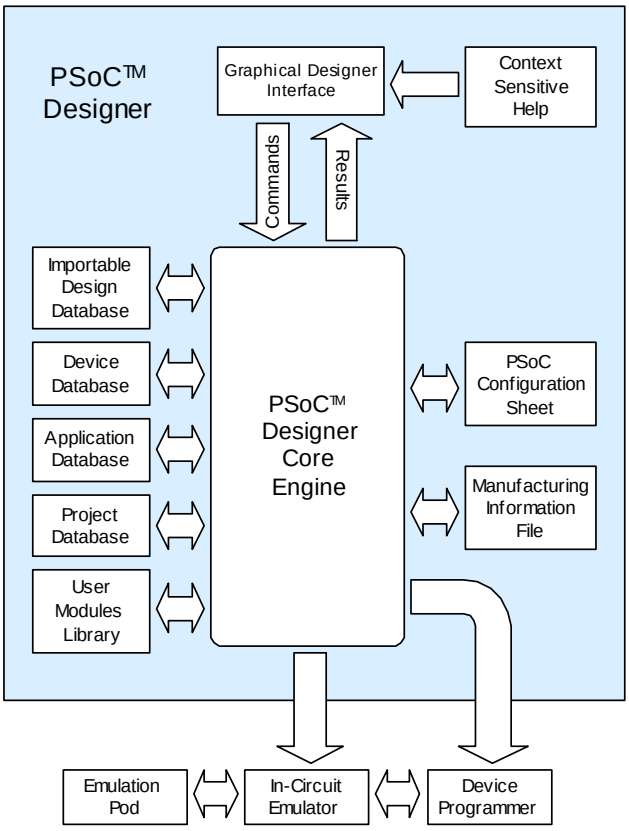
Development Tools

PSoC Designer is a Microsoft® Windows®-based, integrated development environment for the enCoRe III LV. The PSoC Designer IDE and application runs on Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP. (Refer Figure 3)

PSoC Designer helps the customer to select an operating configuration, write application code that uses the enCoRe III LV, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.

Figure 3. PSoC Designer Subsystems



PSoC Designer Software Subsystems

Device Editor

The device editor subsystem enables the user to select different on-board analog and digital components called user modules using the blocks. Examples of user modules are ADCs, PWMs, and SPI.

PSoC Designer sets up power on initialization tables for selected block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. After the framework is generated, the user can add application-specific code to flesh out the framework. It is also possible to change the selected components and regenerate the framework.

Application Editor

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

Assembler. The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler that supports the enCoRe III LV family of devices is available. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs.

The embedded, optimizing C compiler provides all the features of C tailored to the enCoRe III LV architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, enabling designers to test the program in a physical system while providing an internal view of the device. Debugger commands allow the designer to read the program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with enCoRe III LV, enCoRe III, and all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the enCoRe III LV device in the target board and performs full speed (12 MHz) operation.

Designing with User Modules

The development process for the enCoRe III LV device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks provide a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources have the ability to implement a wide variety of user-selectable functions. Each block has several registers that determine its function and connectivity to other blocks, multiplexers, buses and to the IO pins. Iterative development cycles permit you to adapt the hardware and software. This substantially lowers the risk of having to select a different part to meet the final design requirements.

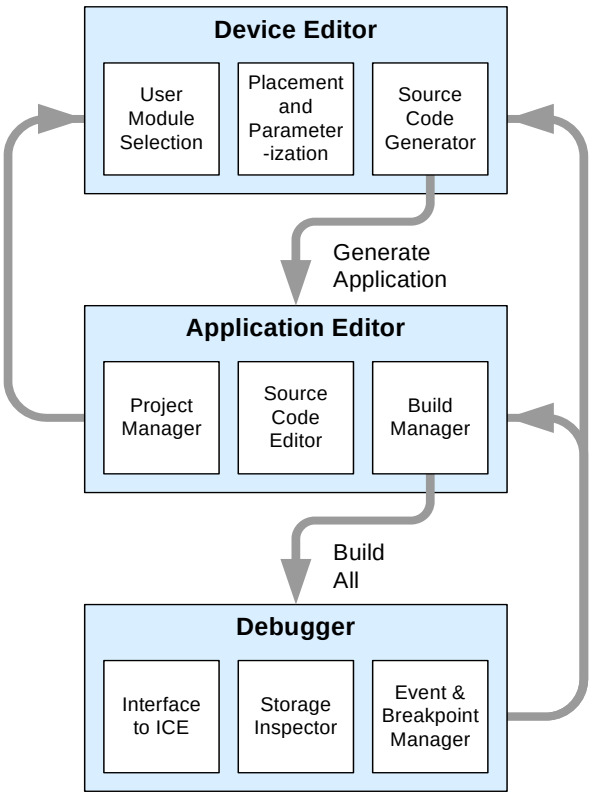
To speed the development process, the PSoC Designer Integrated Development Environment (IDE) provides a library of prebuilt, pretested hardware peripheral functions, called “User Modules.” User Modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties. The standard User Module library contains seven common peripherals such as ADCs, SPI, I2C and PWMs to configure the enCoRe III LV peripherals.

Each user module establishes the basic register settings that implement the selected function. It also provides parameters that allow you to tailor its precise configuration to your particular application. For example, a Pulse Width Modulator User Module configures a digital enCoRe III LV block for 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. User modules also provide tested software to cut your development time. The user module application programming interface (API) provides high-level functions to control and respond to hardware events at run time. The API also provides optional interrupt service routines that you can adapt as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

The development process starts when you open a new project and bring up the Device Editor, a graphical user interface (GUI) for configuring the hardware. You pick the user modules you need for your project and map them onto the enCoRe III LV blocks with point-and-click simplicity. Next, you build signal chains by interconnecting user modules to each other and the IO pins. At this stage, you also configure the clock source connections and enter parameter values directly or by selecting values from drop-down menus. When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high-level user module API functions.

Figure 4. User Module and Source Code Development Flows



The next step is to write your main program, and any subroutines using PSoC Designer’s Application Editor subsystem. The Application Editor includes a Project Manager that allows you to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for both C and assembly language. File search capabilities include simple string searches and recursive “grep-style” patterns. A single mouse click invokes the Build Manager. It employs a professional-strength “makefile” system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project-level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double clicking the error message takes you directly to the offending line of source code. When all is correct, the linker builds a HEX file image suitable for programming.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Table 2. Acronyms Used

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
GUI	graphical user interface
HBM	human body model
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
IO	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PLL	phase-locked loop
POR	power on reset
PPOR	precision power on reset
PSoC	Programmable System-on-Chip™
PWM	pulse width modulator
SC	switched capacitor
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 8 on page 15 lists all the abbreviations used to measure the enCoRe III LV devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (e.g., 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimal.

Pin Information

The enCoRe III LV device is available in 28-pin SSOP and 32-pin QFN packages, which are listed and shown in the following tables. Every port pin (labeled with a “P”) is capable of Digital IO and connection to the common analog bus. However, Vss, Vdd, SMP, and XRES are not capable of Digital IO.

28-Pin Part Pinout

Figure 5. CY7C60323-PVXC 28-Pin Device

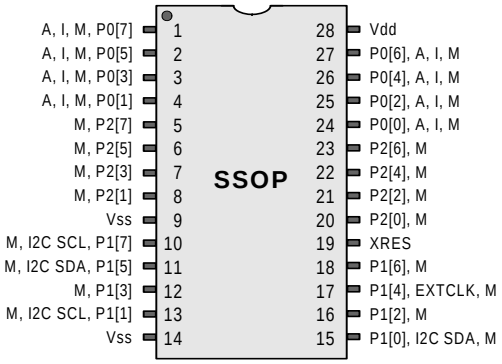


Table 3. Pin Definitions - CY7C60323-PVXC 28-Pin Device

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I, M	P0[7]	Analog Column Mux Input.
2	IO	I, M	P0[5]	Analog Column Mux Input and Column Output.
3	IO	I, M	P0[3]	Analog Column Mux Input and Column Output, Integrating Input.
4	IO	I, M	P0[1]	Analog Column Mux Input, Integrating Input.
5	IO	M	P2[7]	
6	IO	M	P2[5]	
7	IO	I, M	P2[3]	Direct Switched Capacitor Block Input.
8	IO	I, M	P2[1]	Direct Switched Capacitor Block Input.
9	Power		Vss	Ground Connection.
10	IO	M	P1[7]	I2C Serial Clock (SCL).
11	IO	M	P1[5]	I2C Serial Data (SDA).
12	IO	M	P1[3]	
13	IO	M	P1[1]	I2C Serial Clock (SCL), ISSP-SCLK.
14	Power		Vss	Ground Connection.
15	IO	M	P1[0]	I2C Serial Data (SDA), ISSP-SDATA.
16	IO	M	P1[2]	
17	IO	M	P1[4]	Optional External Clock Input (EXTCLK).
18	IO	M	P1[6]	
19	Input		XRES	Active HIGH External Reset with Internal Pull Down.
20	IO	I, M	P2[0]	Direct Switched Capacitor Block Input.
21	IO	I, M	P2[2]	Direct Switched Capacitor Block Input.
22	IO	M	P2[4]	
23	IO	M	P2[6]	
24	IO	I, M	P0[0]	Analog Column Mux Input.

Table 3. Pin Definitions - CY7C60323-PVXC 28-Pin Device (continued)

Pin No.	Type		Name	Description
	Digital	Analog		
25	IO	I, M	P0[2]	Analog Column Mux Input.
26	IO	I, M	P0[4]	Analog Column Mux Input.
27	IO	I, M	P0[6]	Analog Column Mux Input.
28	Power		Vdd	Supply Voltage.

LEGEND A: Analog, I: Input, O = Output, and M = Analog Mux Input.

32-Pin Part Pinout

Figure 6. CY7C60323-LFXC 32-Pin Device

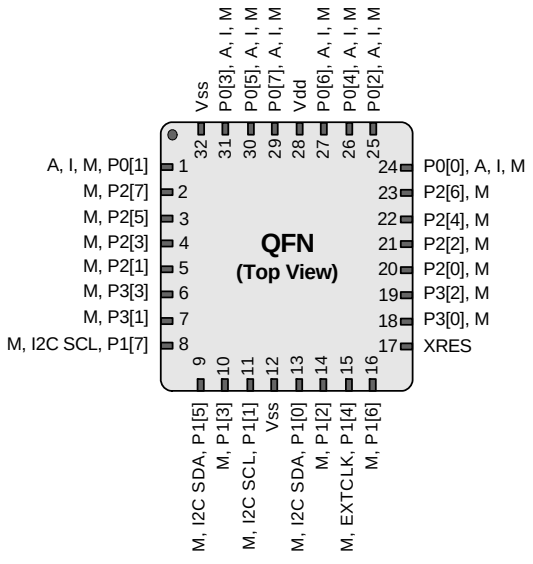


Figure 7. CY7C60333-LFXC 32-Pin Device

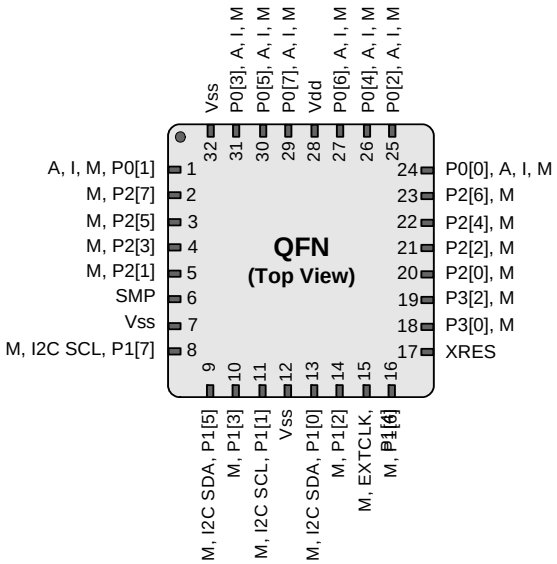


Figure 8. CY7C60323-LTXC 32-Pin Device

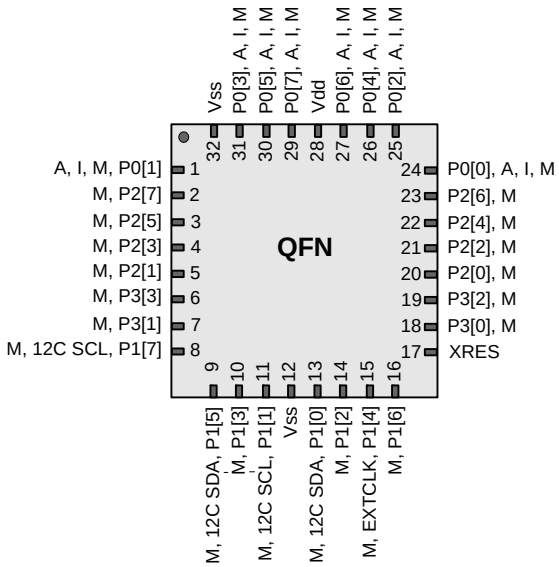


Figure 9. CY7C60333-LTXC 32-Pin Device

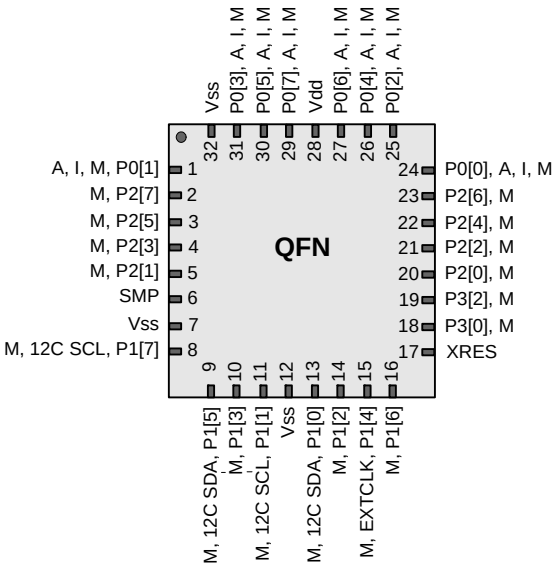


Table 4. 32-Pin Part Pinout (QFN*)

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I, M	P0[1]	Analog Column Mux Input, Integrating Input.
2	IO	M	P2[7]	
3	IO	M	P2[5]	
4	IO	M	P2[3]	
5	IO	M	P2[1]	
6	IO	M	P3[3]	In CY7C60323 Part.
6	Power		SMP	Switch Mode Pump (SMP) Connection to required external components in CY7C60333 Part.
7	IO	M	P3[1]	In CY7C60323 Part.
7	Power		Vss	Ground Connection in CY7C60333 Part.
8	IO	M	P1[7]	I2C Serial Clock (SCL).
9	IO	M	P1[5]	I2C Serial Data (SDA).
10	IO	M	P1[3]	
11	IO	M	P1[1]	I2C Serial Clock (SCL), ISSP-SCLK.
12	Power		Vss	Ground Connection.
13	IO	M	P1[0]	I2C Serial Data (SDA), ISSP-SDATA.
14	IO	M	P1[2]	
15	IO	M	P1[4]	Optional External Clock Input (EXTCLK).
16	IO	M	P1[6]	
17	Input		XRES	Active HIGH External Reset with Internal Pull Down.
18	IO	M	P3[0]	
19	IO	M	P3[2]	
20	IO	M	P2[0]	
21	IO	M	P2[2]	
22	IO	M	P2[4]	
23	IO	M	P2[6]	
24	IO	I, M	P0[0]	Analog Column Mux Input.
25	IO	I, M	P0[2]	Analog Column Mux Input.
26	IO	I, M	P0[4]	Analog Column Mux Input.
27	IO	I, M	P0[6]	Analog Column Mux Input.
28	Power		Vdd	Supply Voltage.
29	IO	I, M	P0[7]	Analog Column Mux Input.
30	IO	I, M	P0[5]	Analog Column Mux Input.
31	IO	I, M	P0[3]	Analog Column Mux Input, Integrating Input.
32	Power		Vss	Ground Connection.

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.
* The QFN package has a center pad that must be connected to ground (Vss).

Register Reference

This section lists the registers of the enCoRe III LV device. For detailed register information, refer the *PSoC Mixed-Signal Array Technical Reference Manual*.

Register Conventions

The register conventions specific to this section are listed in Table 5.

Table 5. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The enCoRe III LV device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 6. Register Map 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASE10CR0	80	RW		C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASE11CR0	84	RW		C4	
PRT1IE	05	RW		45			85			C5	
PRT1GS	06	RW		46			86			C6	
PRT1DM2	07	RW		47			87			C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
PRT3DR	0C	RW		4C			8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW		4E			8E			CE	
PRT3DM2	0F	RW		4F			8F			CF	
	10			50			90		CUR_PP	D0	RW
	11			51			91		STK_PP	D1	RW
	12			52			92			D2	
	13			53			93		IDX_PP	D3	RW
	14			54			94		MVR_PP	D4	RW
	15			55			95		MVW_PP	D5	RW
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 6. Register Map 0 Table: User Space (continued)

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W	AMUXCFG	61	RW		A1		INT_MSK1	E1	RW
DBB00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBB00CR0	23	#		63			A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4			E4	
DBB01DR1	25	W		65			A5			E5	
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#	ADC0_CR	68	#		A8			E8	
DCB02DR1	29	W	ADC1_CR	69	#		A9			E9	
DCB02DR2	2A	RW		6A			AA			EA	
DCB02CR0	2B	#		6B			AB			EB	
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC			EC	
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD			ED	
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_D	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 7. Register Map 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5		ADC0_TR	E5	RW
DBB01OU	26	RW	AMD_CR1	66	RW		A6		ADC1_TR	E6	RW
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B		CLK_CR3	6B	RW		AB		ECO_TR	EB	W

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 7. Register Map 1 Table: Configuration Space (continued)

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_CR	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the enCoRe III LV device. For the most up to date electrical specifications, check the latest data sheet by visiting the web at http://www.cypress.com.

Specifications are valid for 0°C ≤ T_A ≤ 70°C and T_J ≤ 85°C as specified, except where noted.

Refer to Table 20 on page 22 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 10. Voltage versus CPU Frequency

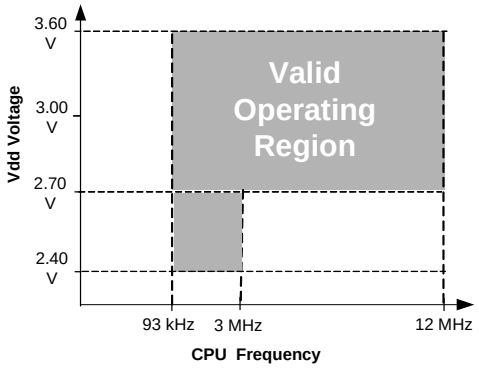
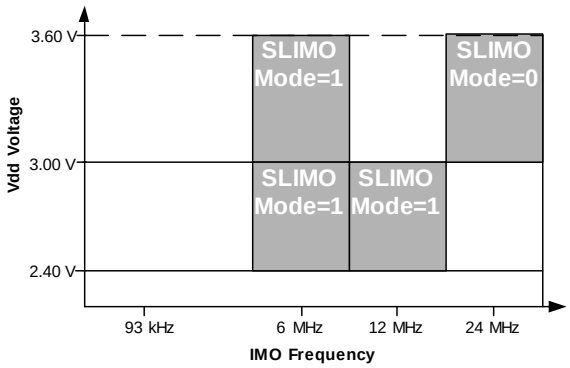


Figure 11. IMO Frequency Trim Options



The allowable CPU operating region for 12 MHz has been extended down to 2.7V from the original 3.0V design target. The customer's application is responsible for monitoring voltage and throttling back CPU speed in accordance with Figure 10 when voltage approaches 2.7V. Refer to Table 18 for LVD specifications. Note that the device does not support a preset trip at 2.7V. To detect Vdd drop at 2.7V, an external circuit or device such as the WirelessUSB LP - CYRF6936 must be employed; or if the design permits, the nearest LVD trip value at 2.9V can be used.

Table 8 lists the units of measure that are used in this section.

Table 8. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatts
dB	decibels	mA	milliampere
fF	femtofarad	ms	millisecond
Hz	hertz	mV	millivolts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	W	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolts	s	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

Absolute Maximum Ratings

Table 9. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage Temperature	–40	–	+90	°C	Higher storage temperatures reduce data retention time.
T_A	Ambient Temperature with Power Applied	0	–	+70	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	–0.5	–	5	V	
V_{IO}	DC Input Voltage	Vss – 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss – 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	–25	–	+25	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up Current	–	–	200	mA	

Operating Temperature

Table 10. Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_A	Ambient Temperature	0	–	+70	°C	
T_J	Junction Temperature	0	–	+85	°C	The temperature rise from ambient to junction is package specific. See Table 33 on page 30. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

Table 11 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, or 2.4V to 3.0V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 11. DC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
Vdd	Supply Voltage	2.40	–	3.6	V	See Table 18 on page 20.
I_{DD3}	Supply Current, IMO = 6 MHz using SLIMO mode.	–	1.2	2	mA	Conditions are Vdd = 3.3V, T_A = 25°C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz.
I_{DD27}	Supply Current, IMO = 6 MHz using SLIMO mode.	–	1.1	1.5	mA	Conditions are Vdd = 2.55V, T_A = 25°C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz.
I_{SB27}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4.	µA	Vdd = 2.55V, 0°C ≤ T_A ≤ 40°C.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	Vdd = 3.3V, 0°C ≤ T_A ≤ 70°C.
V_{REF}	Reference Voltage (Bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate Vdd. Vdd = 3.0V to 3.6V.
V_{REF27}	Reference Voltage (Bandgap)	1.16	1.30	1.33	V	Trimmed for appropriate Vdd. Vdd = 2.4V to 3.0V.
AGND	Analog Ground	V_{REF} – 0.003	V_{REF}	V_{REF} + 0.003	V	

DC General Purpose IO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, or 2.4V to 3.0V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 12. 3.3V DC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd – 1.0	–	–	V	I_{OH} = 3 mA, V_{DD} > 3.0V
V_{OL}	Low Output Level	–	–	0.75	V	I_{OL} = 10 mA, V_{DD} > 3.0V
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 3.6.
V_{IH}	Input High Level	2.1	–		V	Vdd = 3.0 to 3.6.
V_H	Input Hysteresis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

Table 13. 2.7V DC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd – 0.4	–	–	V	I_{OH} = 2.5 mA (6.25 Typ), V_{DD} = 2.4 to 3.0V (16 mA maximum, 50 mA Typ combined I_{OH} budget).
V_{OL}	Low Output Level	–	–	0.75	V	I_{OL} = 10 mA, V_{DD} = 2.4 to 3.0V (90 mA maximum combined I_{OL} budget).
V_{IL}	Input Low Level	–	–	0.75	V	Vdd = 2.4 to 3.0.
V_{IH}	Input High Level	2.0	–	–	V	Vdd = 2.4 to 3.0.
V_H	Input Hysteresis	–	90	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, or 2.4V to 3.0V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 14. 3.3V DC Operational Amplifier Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OSOA}	Input Offset Voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	10	–	µV/°C	
I_{EBOA}[1]	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0	–	Vdd – 1	V	
G_{OLOA}	Open Loop Gain	–	80	–	dB	
I_{SOA}	Amplifier Supply Current	–	10	30	µA	

Table 15. 2.7V DC Operational Amplifier Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OSOA}	Input Offset Voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	10	–	µV/°C	
I_{EBOA}[1]	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0	–	Vdd – 1	V	
G_{OLOA}	Open Loop Gain	–	80	–	dB	
I_{SOA}	Amplifier Supply Current	–	10	30	µA	

Note
1. Atypical behavior: I_{EBOA} of Port 0 Pin 0 is below 1 nA at 25°C; 50 nA over temperature. Use Port 0 Pins 1–7 for the lowest leakage of 200 nA.

DC Switch Mode Pump Specifications

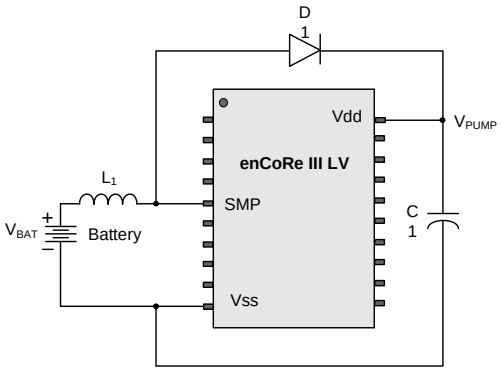
Table 16 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, or 2.4V to 3.0V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 16. DC Switch Mode Pump (SMP) Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{PUMP3V}	3.3V Output Voltage from Pump	3.00	3.25	3.60	V	Configuration of footnote.[2] Average, neglecting ripple. SMP trip voltage is set to 3.25V.
V_{PUMP2V}	2.6V Output Voltage from Pump	2.45	2.55	2.80	V	Configuration of footnote.[2] Average, neglecting ripple. SMP trip voltage is set to 2.55V.
I_{PUMP}	Available Output Current V_{BAT} = 1.5V, V_{PUMP} = 3.25V V_{BAT} = 1.3V, V_{PUMP} = 2.55V	 8 8	 – –	 – –	 mA mA	Configuration of footnote.[2] SMP trip voltage is set to 3.25V. SMP trip voltage is set to 2.55V.
V_{BAT3V}	Input Voltage Range from Battery	1.0	–	3.3	V	Configuration of footnote.[2] SMP trip voltage is set to 3.25V.
V_{BAT2V}	Input Voltage Range from Battery	1.0	–	2.8	V	Configuration of footnote.[2] SMP trip voltage is set to 2.55V.
$V_{BATSTART}$	Minimum Input Voltage from Battery to Start Pump	1.2	–	–	V	Configuration of footnote.[2] 0°C ≤ T_A ≤ 100. 1.25V at T_A = –40°C.
ΔV_{PUMP_Line}	Line Regulation (over Vi range)	–	5	–	$\%V_O$	Configuration of footnote.[2] V_O is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 18 on page 20.
ΔV_{PUMP_Load}	Load Regulation	–	5	–	$\%V_O$	Configuration of footnote.[2] V_O is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 18 on page 20.
ΔV_{PUMP_Ripple}	Output Voltage Ripple (depends on cap/load)	–	100	–	mVpp	Configuration of footnote.[2] Load is 5 mA.
E_3	Efficiency	35	50	–	%	Configuration of footnote.[2] Load is 5 mA. SMP trip voltage is set to 3.25V.
E_2	Efficiency	35	80	–	%	For I load = 1 mA, V_{PUMP} = 2.55V, V_{BAT} = 1.3V, 10 µH inductor, 1 µF capacitor, and Schottky diode.
F_{PUMP}	Switching Frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching Duty Cycle	–	50	–	%	

Note
2. L_1 = 2 µH inductor, C_1 = 10 µF capacitor, D_1 = Schottky diode. See Figure 12 on page 20.

Figure 12. Basic Switch Mode Pump Circuit



DC Analog Mux Bus Specifications

Table 17 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, or 2.4V to 3.0V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 17. DC Analog Mux Bus Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{SW}	Switch Resistance to Common Analog Bus	–	–	400 800	Ω Ω	Vdd ≥ 2.7V 2.4V ≤ Vdd ≤ 2.7V
R_{VDD}	Resistance of Initialization Switch to Vdd	–	–	800	Ω	

DC POR and LVD Specifications

Table 18 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, or 2.4V to 3.0V and 00°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 18. DC POR and LVD Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{PPOR0} V_{PPOR1}	Vdd Value for PPOR Trip PORLEV[1:0] = 00b PORLEV[1:0] = 01b	–	2.36 2.82	2.40 2.95	V V	Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[3]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[4]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD37}	VM[2:0] = 011b	3.06	3.13	3.20	V	
	Vdd Value for PUMP Trip					
V_{PUMP0}	VM[2:0] = 000b	2.45	2.55	2.62[5]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[6]	V	

Notes
3. Always greater than 50 mV above VPPOR (PORLEV = 00) for falling supply.
4. Always greater than 50 mV above VPPOR (PORLEV = 01) for falling supply.
5. Always greater than 50 mV above VLVD0.
6. Always greater than 50 mV above VLVD3.

DC Programming Specifications

Table 19 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, or 2.4V to 3.0V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 19. DC Programming Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations	2.70	–	–	V	
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.1	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd – 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[7]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

Note
7. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

AC Electrical Characteristics

AC Chip-Level Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, or 2.4V to 3.0V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 20. 3.3V AC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.4	24	24.6[8, 9]	MHz	Trimmed for 3.3V operation using factory trim values. See Figure 11 on page 15. SLIMO mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.75	6	6.35[8, 9]	MHz	Trimmed for 3.3V operation using factory trim values. See Figure 11 on page 15. SLIMO mode = 1.
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.3[8, 9]	MHz	
F_{BLK33}	Digital Block Frequency (3.3V Nominal)	0	24	24.6[8, 10]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
Jitter32k	32 kHz RMS Period Jitter	–	100	200	ns	
Jitter32k	32 kHz Peak-to-Peak Period Jitter	–	1400	–		
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[9]	MHz	Trimmed. Using factory trim values.
Jitter24M1	24 MHz Peak-to-Peak Period Jitter (IMO)	–	600		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

Table 21. 2.7V AC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{IMO12}	Internal Main Oscillator Frequency for 12 MHz	11.5	12	12.7[8, 11]	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 11 on page 15. SLIMO mode = 1.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.75	6	6.35[8, 11]	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 11 on page 15. SLIMO mode = 1.
F_{CPU1}	CPU Frequency (2.7V Nominal)	0.093	3	3.15[8, 11]	MHz	24 MHz only for SLIMO mode = 0.
F_{BLK27}	Digital Block Frequency (2.7V Nominal)	0	12	12.5[8, 11]	MHz	Refer to the AC Digital Block Specifications.
F_{32K1}	Internal Low Speed Oscillator Frequency	8	32	96	kHz	
Jitter32k	32 kHz RMS Period Jitter	–	150	200	ns	
Jitter32k	32 kHz Peak-to-Peak Period Jitter	–	1400	–		
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

Notes
8. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
9. 3.0V < Vdd < 3.6V.
10. See the individual user module data sheets for information on maximum frequencies for user modules.
11. 2.4V < Vdd < 3.0V.

Figure 13. 24 MHz Period Jitter (IMO) Timing Diagram

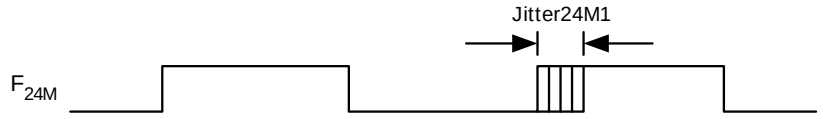
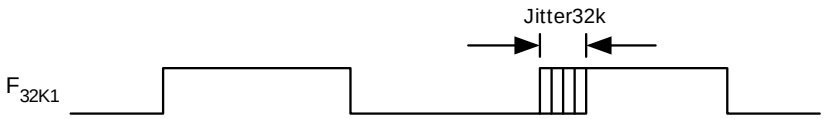


Figure 14. 32 kHz Period Jitter (ILO) Timing Diagram



AC General Purpose IO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, or 2.4V to 3.0V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 3.3V, or 2.7V at 25°C and are for design guidance only.

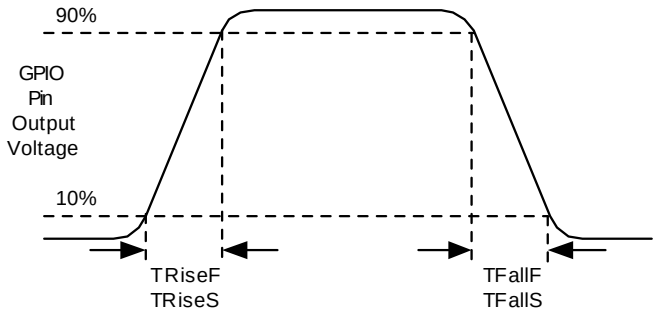
Table 22. 3.3V AC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	Normal Strong Mode
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	7	27	–	ns	Vdd = 3 to 3.6V, 10%–90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	7	22	–	ns	Vdd = 3 to 3.6V, 10%–90%

Table 23. 2.7V AC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	3	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	6	–	50	ns	Vdd = 2.4 to 3.0V, 10%–90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	6	–	50	ns	Vdd = 2.4 to 3.0V, 10%–90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	18	40	120	ns	Vdd = 2.4 to 3.0V, 10%–90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	18	40	120	ns	Vdd = 2.4 to 3.0V, 10%–90%

Figure 15. GPIO Timing Diagram



AC Operational Amplifier Specifications

Table 24 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, or 2.4V to 3.0V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 24. AC Operational Amplifier Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{COMP}	Comparator Mode Response Time, 50 mV Overdrive			100 200	ns ns	Vdd ≥ 3.0V. 2.4V < Vcc < 3.0V.

AC Analog Mux Bus Specifications

Table 25 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, or 2.4V to 3.0V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 25. AC Analog Mux Bus Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{SW}	Switch Rate	–	–	3.17	MHz	

AC Digital Block Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, or 2.4V to 3.0V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 26. 3.3V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All Functions	Maximum Block Clocking Frequency (< 3.6V)			24.6	MHz	3.0V < Vdd < 3.6V.
Timer/ Counter/ PWM	Enable Pulse Width	50[12]	–	–	ns	
	Maximum Frequency	–	–	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50	–	–	ns	
	Disable Mode	50	–	–	ns	
	Maximum Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	50	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.

Note
12. 50 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

AC External Clock Specifications

Table 27. 2.7V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All Functions	Maximum Block Clocking Frequency			12.7	MHz	2.4V < Vdd < 3.0V.
Timer/ Counter/ PWM	Enable Pulse Width	100	–	–	ns	
	Maximum Frequency	–	–	12.7	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	100	–	–	ns	
	Disable Mode	100	–	–	ns	
	Maximum Frequency	–	–	12.7	MHz	
SPIM	Maximum Input Clock Frequency	–	–	6.35	MHz	Maximum data rate at 3.17 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	100	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	12.7	MHz	Maximum data rate at 1.59 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	12.7	MHz	Maximum data rate at 1.59 MHz due to 8 x over clocking.

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 28. 3.3V AC External Clock Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

Table 29. 2.7V AC External Clock Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1	0.093	–	3.08	MHz	Maximum CPU frequency is 3 MHz at 2.7V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater	0.186	–	6.35	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High Period with CPU Clock divide by 1	160	–	5300	ns	
–	Low Period with CPU Clock divide by 1	160	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

AC Programming Specifications

Table 30 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 30. AC Programming Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	15	–	ms	
T_{WRITE}	Flash Block Write Time	–	30	–	ms	
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 ≤ Vdd ≤ 3.6
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	–	–	70	ns	2.4 ≤ Vdd ≤ 3.0

AC I²C Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 3.6V and 0°C ≤ T_A ≤ 70°C, or 2.4V to 3.0V and 0°C ≤ T_A ≤ 70°C, respectively. Typical parameters apply to 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 31. AC Characteristics of the I²C SDA and SCL Pins for Vdd ≥ 3.0V

Parameter	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Set up Time for a Repeated START Condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs
$T_{SUDATI2C}$	Data Set up Time	250	–	100[13]	–	ns
$T_{SUSTOI2C}$	Set up Time for STOP Condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns

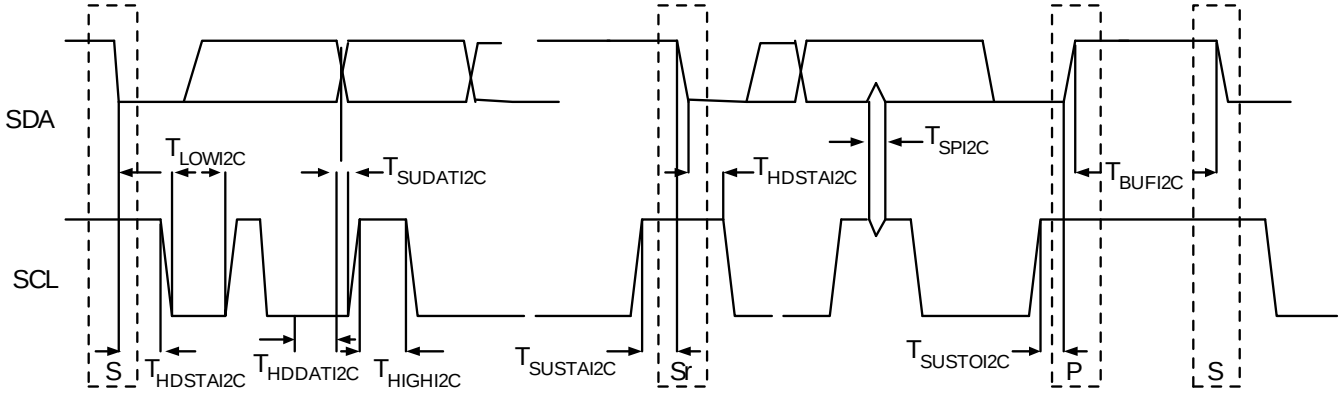
Table 32. 2.7V AC Characteristics of the I²C SDA and SCL Pins (Fast Mode not Supported)

Parameter	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency	0	100	–	–	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	–	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	–	–	µs
$T_{SUSTAI2C}$	Set up Time for a Repeated START Condition	4.7	–	–	–	µs
$T_{HDDATI2C}$	Data Hold Time	0	–	–	–	µs
$T_{SUDATI2C}$	Data Set up Time	250	–	–	–	ns
$T_{SUSTOI2C}$	Set up Time for STOP Condition	4.0	–	–	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	–	–	µs
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	–	–	ns

Note

13. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT}$ ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Figure 16. Definition for Timing for Fast/Standard Mode on the I²C Bus



Packaging Information

This section illustrates the packaging specifications for the CY7C603xx device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/support.

Packaging Dimensions

Figure 17. 28-Pin (210-Mil) SSOP

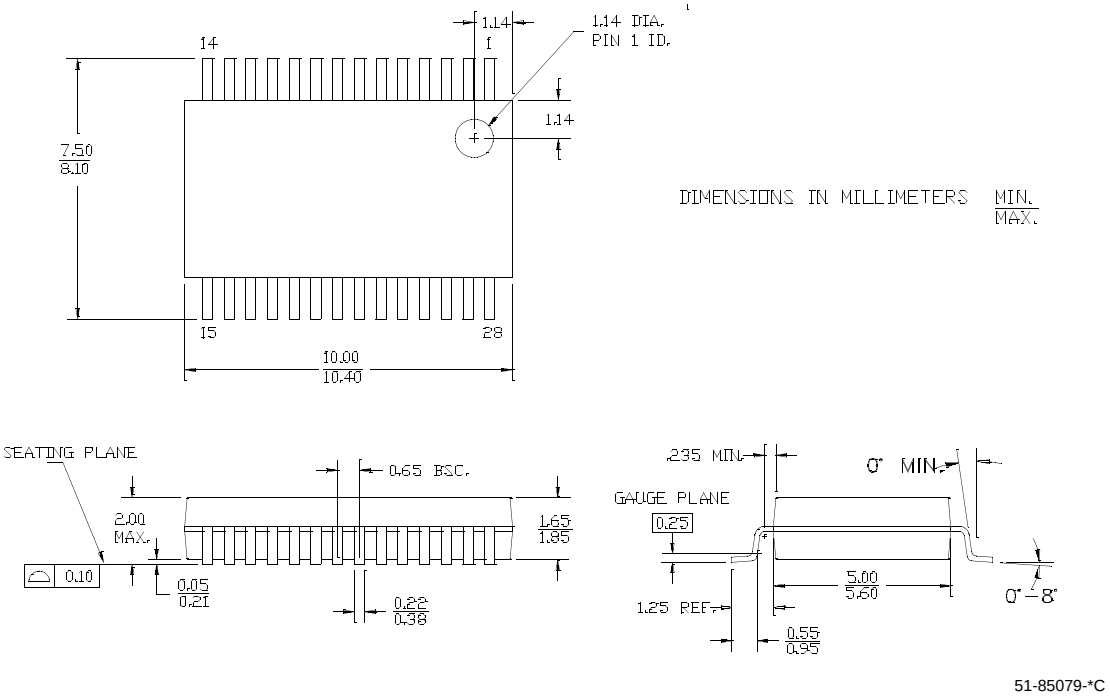


Figure 18. 32-Pin QFN (5 x 5 mm)

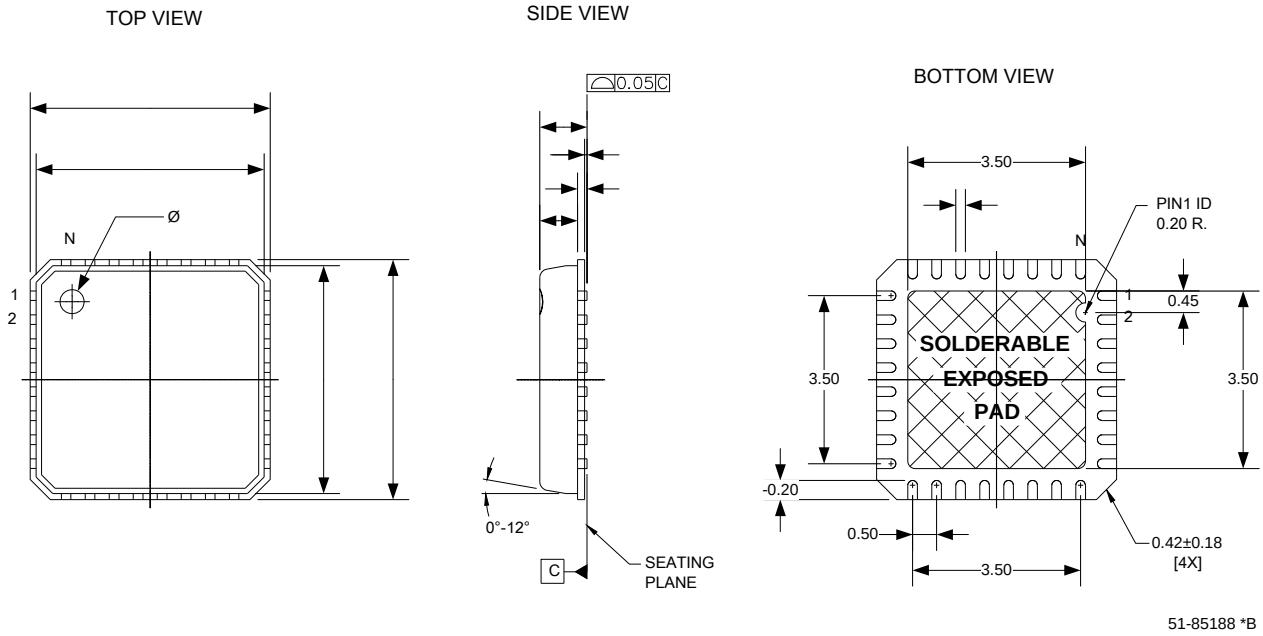
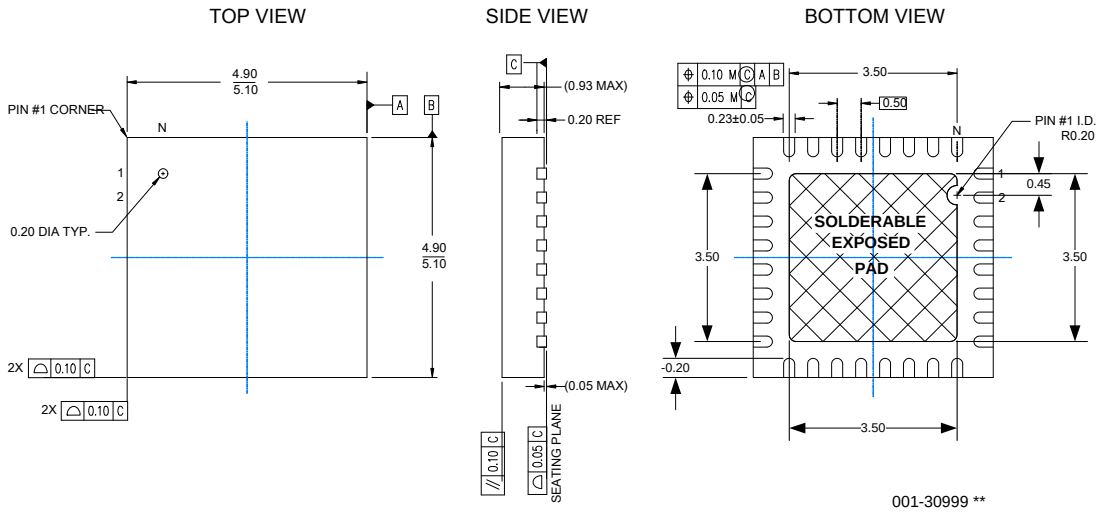


Figure 19. 32-Pin QFN (5 x 5 mm) (Sawn)



Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Thermal Impedances

Table 33. Thermal Impedances per Package

Package	Typical θ_{JA} *	Typical θ_{JC}
28 SSOP	96 °C/W	39 °C/W
32 QFN	22 °C/W	12 °C/W

* $T_J = T_A + \text{Power} \times \theta_{JA}$

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 34. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature*	Maximum Peak Temperature
28 SSOP	240°C	260°C
32 QFN	240°C	260°C

*Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220±5°C with Sn-Pb or 245±5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Ordering Information

The following table lists the CY7C603xx device's key package features and ordering codes.

Table 35. CY7C603xx Device Key Features and Ordering Information

Ordering Part Number	Flash Size	RAM Size	SMP	IO	Package Type
CY7C60323-PVXC	8K	512	No	24	28-SSOP
CY7C60323-PVXCT	8K	512	No	24	28-SSOP Tape and Reel
CY7C60323-LFXC	8K	512	No	28	32-QFN
CY7C60323-LFXCT	8K	512	No	28	32-QFN Tape and Reel
CY7C60323-LTXC	8K	512	No	28	32-QFN Sawn
CY7C60323-LTXCT	8K	512	No	28	32-QFN Sawn Tape and Reel
CY7C60333-LFXC	8K	512	Yes	26	32-QFN
CY7C60333-LFXCT	8K	512	Yes	26	32-QFN Tape and Reel
CY7C60333-LTXC	8K	512	Yes	26	32-QFN Sawn
CY7C60333-LTXCT	8K	512	Yes	26	32-QFN Sawn Tape and Reel

Document History Page

Description Title: CY7C603xx, enCoRe™ III Low Voltage Document Number: 38-16018				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	339394	See ECN	BON	New Advance Data Sheet
*A	399556	See ECN	BHA	Changed from Advance Information to Preliminary. Changed data sheet format. Removed CY7C604xx.
*B	461240	See ECN	TYJ	Modified Figure 10 to include 2.7V Vdd at 12 MHz operation
*C	470485	See ECN	TYJ	Corrected part numbers in section 4 to match with part numbers in Ordering Information. From CY7C60323-28PVXC, CY7C60323-56LFXC and CY7C60333-56LFXC to CY7C60323-PVXC, CY7C60323-LFXC and CY7C60333-LFXC respectively Changed from Preliminary to final data sheet
*D	513713	See ECN	KKVTMP	Change title from Wireless enCoRe II to enCoRe III Low Voltage Applied new template formatting
*E	2197567	See ECN	UVS/AESA	Added 32-Pin Sawn QFN Pin Diagram, package diagram, and ordering information.